In the Claims:

Please amend the claims as indicated below.

1. (Currently amended) Apparatus for processing a differential input signal, the apparatus comprising

a peak detector with a differential input, the peak detector configured to provide ~~providing~~ a first voltage being proportional to an average voltage peak at the peak detector's differential input,

a compressor configured to process ~~processing~~ the first voltage in order to provide a second voltage,

a voltage controllable current source configured to provide ~~providing~~ a trim current being adjustable by the second voltage,

a hysteresis equipped circuit having ~~whose~~ hysteresis characteristics, the hysteresis equipped circuit configured to adjust the hysteresis circuit responsive to ~~are adjustable by~~ the trim current,

wherein the peak detector is operationally coupled to the compressor and the compressor is operationally coupled to the voltage controllable current source.

2. (Previously presented)The apparatus of claim 1, wherein the peak detector comprises an integrator.

3. (Previously presented)The apparatus of claim 1, wherein the peak detector operates on the envelop of a differential input signal being applied to the differential input.

4. (Previously presented)The apparatus of claim 1, wherein the peak detector is designed to constantly follow the average voltage peak at the peak detector's differential input.

5. (Previously presented) The apparatus of claim 1, providing a hysteresis characteristics depending on the average voltage peak at the peak detector's differential input.

6. (Previously presented) The apparatus of claim 1, wherein the peak detector comprises a differential input transistor pair at its differential input.

7. (Previously presented) The apparatus of claim 6, wherein the load conditions of the differential input transistor pair changes when the average voltage peak changes.

8. (Previously presented) The apparatus of claim 1, wherein the hysteresis characteristics are adjusted by shifting trip-levels of the hysteresis equipped circuit to lower levels if the differential input signal is a low level signal and to higher levels if the differential input signal is a high level signal.

9. (Previously presented)The apparatus of claim 1, wherein a differential clock signal is used as the differential input signal to perform a sensing phase and an appropriate adjustment of the hysteresis characteristics.

10. (Previously presented) The apparatus of claim 1, wherein the compressor applies a function when processing the first voltage (42) in order to provide the second voltage.

11. (Currently amended) Control circuitry for a display system comprising an array of interfaces, whereby at least one interface comprises

a peak detector with a differential input, the peak detector configured to provide ~~providing~~ a first voltage being proportional to an average voltage peak of a differential clock signal being applied to the peak detector's differential input,

a compressor configured to process ~~processing~~ the first voltage in order to provide a second voltage,

a voltage controllable current source configured to provide ~~providing~~ a current being adjustable by the second voltage,

a hysteresis equipped circuit having ~~whose~~ hysteresis characteristics, the hysteresis equipped circuit configured to adjust the hysteresis circuit responsive to ~~are adjustable by~~ the current.

12. (Previously presented)The control circuitry of claim 11, wherein a signal is provided by the at least one interface (62.1) to other interfaces of the array of interfaces in order to allow the hysteresis characteristics of the other interfaces to be adjusted, too.

13. (Previously presented) The control circuitry of claim 11, wherein the interfaces of the array of interfaces serve as differential RSDS interfaces.

14. (Previously presented) The control circuitry of claim 11, wherein the interfaces of the array of interfaces serve as low EMI/low power interfaces between timing controllers and digital-to-analog latches employed for driving analog signals onto column electrodes of a display panel of the display system.

15. (Previously presented)The control circuitry of claim 11 further comprising a transmitting circuit for transmitting video data to the array of interfaces.

16. (Previously presented) The control circuitry of claim 15, wherein the array of interfaces converts the video data into analog signals for driving onto column electrodes of a display panel of the display system.

17. (Previously presented)The control circuitry of claim 14, wherein any kind of reduced swing signaling can be used to transmit the video data to the array of interfaces.